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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/923,720	08/06/2001	Frank Pietzschmann	2000P15141	1125

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EXAMINER	
CHAN, EMILY Y	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 03/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n N .	Applicant(s)	
	09/923,720	PIETZSCHMANN, FRANK	
	Examin r	Art Unit	
	emily y chan	2829	9

-- The MAILING DATE of this communication appears on th cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *CFRfiled on 12-17-01* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *17-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 9 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

El ction/R strictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-16, drawn to semiconductor integrated circuit test apparatus, classified in class 324, subclass 756

II. Claims 17-26, drawn to a method of testing semiconductor circuit, classified in class 324, subclass 758.

The inventions are distinct, each from the other because:

Inventions II and I are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case, the process as claimed can be practiced by another materially different apparatus such as an probe apparatus operates to test the electrical characteristics of the semiconductor integrated circuit by supplying a high frequency test signal from the test head to the semiconductor integrated circuit on the wafer through probe card in response to a command from a tester and does not required the control circuitry detail included in the probe card.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

During a telephone conversation with Mr. Greenberg on 3-11-03 a provisional election was made without traverse to prosecute the invention of I, claims 1-16. Affirmation of this election must be made by applicant in replying to this Office action. Claims 17-26 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claims 1-16 are presented for examination.

Specification

The disclosure is objected to because of the following informalities: On page 7, line 5, two "also"s are recited and one should deleted. On page 17, line 24, the recitation "inventioal7" is unclear. On page 25, "Fig. 4" should be " Fig. 4A", and "Fig. 4A" should be "Fig. 4B". Appropriate correction is required.

Drawings

The drawing 1 is objected to because planarizer 7 is not shown on Fig 1. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim1 is objected to because of the following informalities: in claim 1, the recitation "said contacts in direction substantially orthogonal to the wafer surface profile" is unclear. Mainly it is unclear whether the "contacts" belong to the semiconductor integrated circuit or to the probe card. The examiner assumes it is probe card 's "contacts". In claim 5, the recitation " connected to said contacts and to said substrate"

is unclear. It is unclear whether the "contacts" belong to the semiconductor integrated circuit or to the probe card. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 7-9, 11-12 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hagihara '(192) in view of Itoyama('053).

With respect to claim 1, Hagihara '(192) discloses a test apparatus or a probe card used in probing apparatus (see Fig 2) for testing the electrical characteristics of a semiconductor wafer as claimed, comprising:

a chuck (13)(see col. 5, line 29) for holding a wafer (12) that has at least one semiconductor integrated circuit (semiconductor chips) with a group of contact areas (12b)(see col.5, line 20) that define a wafer surface profile;

a test head (22)(see Fig 1) that is configured opposite the chuck (13)

a probe card (32) that is configured on the test head (22) and that has contact (37) (see col. 7 line4-5) for making contact with the contact area of the integrated circuit (semiconductor chip);

actuators (pushing mechanism 38) that are configured on the probe card (32) for aligning the test surface profile parallel with the wafer surface profile (see Col. 10, lines 47-50) and for changing (pushing) a distance between the performance board (48) and

contacts in direction substantially orthogonal to wafer surface profile (see col. 5, lines 47-49 and Col. 6, lines 60-65).

Hagihara '(192) does not teaches that his test head (22) includes a performance board.

Itoyama('053) disclose a probe apparatus (see Fig 3) and particularly teaches a test head (26) that includes a performance board (31).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporated the teaching of Itoyama('053) ' performance board into Hagihara '(192) 'test head for the purpose of enhancing test precision as disclosed by Itoyama('053) (see Col. 2, line 17).

With respect to claim 2, Hagihara '(192) teaches that his actuators (pushing mechanism (38) are configured between a printed wiring board (48) and the probe card (32) and are connected to the printed wiring board (48) and the probe card (32).

With respect to claim 3, Hagihara '(192) teaches that his actuators (pushing members 39) include at least three actuators (39a)(see Col. 2, lines 61-68).

With respect to claim 4, Hagihara '(192) teaches that his probe card (32) is made of a flexible material (see Col. 6, lines 66-67).

With respect to claim 5, Hagihara '(192) teaches that his probe card (32) includes a substrate (see Fig 5) and his actuators (pushing mechanism 38) are connected to the substrate (see Fig. 2).

With respect to claim 7, Hagihara '(192) teaches that his actuators (pushing mechanism 38) is electromechanical elements.

With respect to claims 8-9, Itoyama ('053) teaches that his performance board (31) is a circuit board having a first group of contacts in a first predefined configuration for making contact with evaluation and control electronics (circuitry in test head 26); and a second group of contacts in a second predefined configuration for making contact with the probe card (32)(see Col. 3, lines 37-38).

With respect to claim 12, Itoyama ('053)'s probe card (32) inherently includes test circuit for applying coordinate test signals to the wafer (see abstract).

With respect to claims 14-15, both Hagihara '(192) and Itoyama ('053)'s probe card includes wafer components.

With respect to claim 16, Hagihara '(192) probe card device inherently includes a second wafer that is configured between the probe card (39) and printed wiring board (48) (see Gig 2).

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hagihara '(192) in view of Itoyama ('053) as applied to claim1 above, and further in view of Momohara ('912).

Hagihara '(192) in view of Itoyama ('053) teach that their wafer has a plurity of groups of contacts.

Hagihara '(192) in view of Itoyama ('053) do not teach that their probe card includes a piurality of partial cards that are separated from each other.

Momohara ('912) disclose probing equipment and expressly teach to include a plurality of partial cards that are separated from each other (see Fig. 1 below).

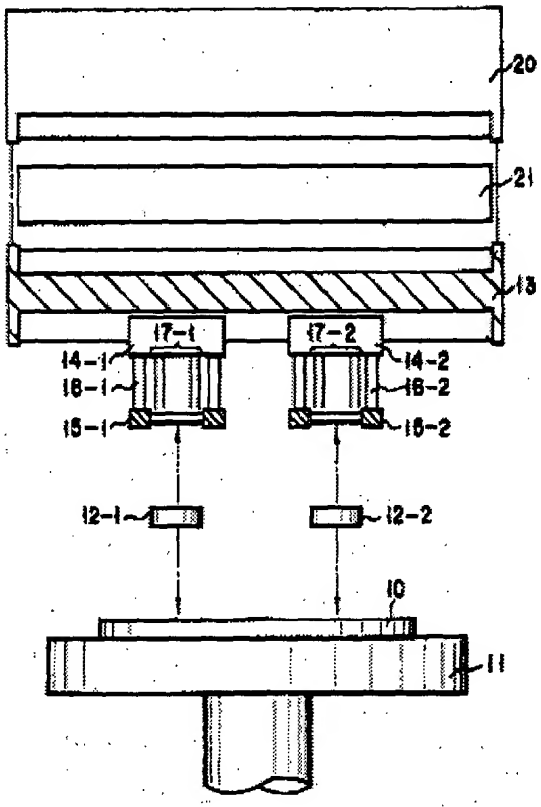


FIG. 1

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporated the teaching of Momohara ('912) 's plurality of partial cards into Hagihara '(192) 'probe card in view of Itoyama ('053) for the purpose of having a high processing ability at a low price disclosed by Momohara ('912) (see Col. 1, lins 66-67).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hagihara '(192) in view of Itoyama ('053) as applied to claim1 above, and further in view of Nagasawa ('083).

Hagihara '(192) in view of Itoyama ('053) do not teach that their probe card has a device for storing and outputting an identification number.

Nagasawa ('083) teaches a probe apparatus and expressly teach a probe card (21) has a device (ROMs 48) for storing and outputting an identification number (the serial number of a probe card).

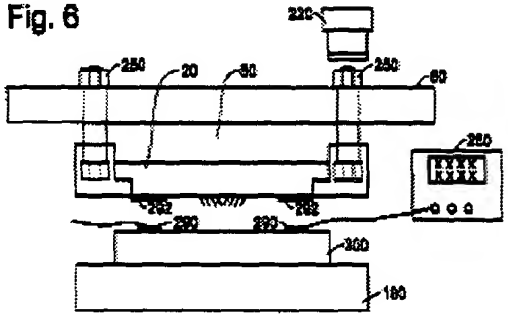
It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporated the teaching of Nagasawa ('083)'s device for storing and outputting an identification number and for applying coordinated signals to the wafer into Hagihara '(192) 'probe card in view of Itoyama ('053) for the purpose of avoiding collision between the probe card and semiconductor disclosed by Nagasawa ('083)(see abstract).

Claims 10 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hagihara '(192) in view of Itoyama ('053) as applied to claim1 above, and further in view of Khoury et al' (629).

Hagihara '(192) in view of Itoyama ('053) do not teach that their probe card has includes distance sensors.

Khoury et al ('629) disclose a probe contact system (see Fig 6 below) and expressly teach a probe card (60) includes distance sensors (gap sensors 292) for determining a distance to the wafer (300) at various points and includes a control device (adjustment device 220) for evaluating the signals from the distance sensors (gap sensors 292) and for driving actuators (50) (see Col. 7, lines 41-65).

Fig. 6



It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporated the teaching of Khoury et al ('629)'s distance sensors into Hagihara '(192) 'probe card device in view of Itoyama ('053) for the purpose of having identical pressure against the surface of the semiconductor wafer when each contacts of probe card contacts with the semiconductor wafer as disclosed by Khoury et al ('629) (see Col. 3, lines 43-45).

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yoon et al disclose a probe card and particularly test circuit (36) included in the probe card (20) (see Fig 2).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to emily y chan whose telephone number is 7033056123. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, cuneo kammie can be reached on 7033081233. The fax phone numbers

for the organization where this application or proceeding is assigned are 7033085841 for regular communications and 7033085841 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 7022056123.

ec
March 20, 2003

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
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